

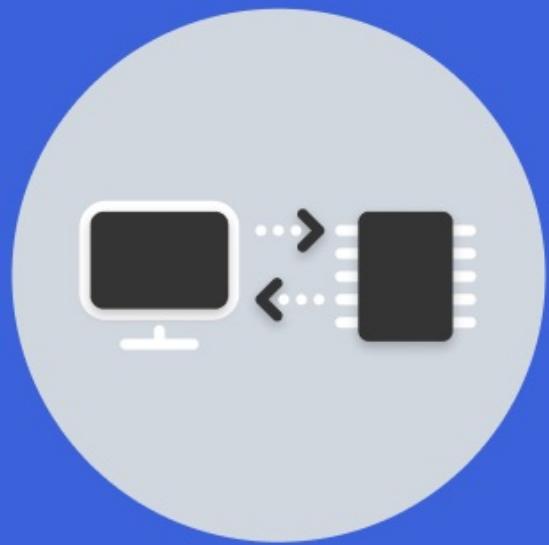


FrontPanel Overview

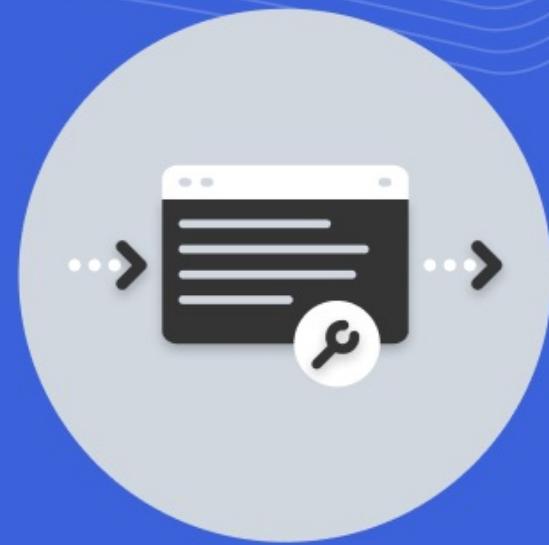
Build high-performance software-connected FPGA applications for prototypes, proof-of-concept, and production

 Opal Kelly

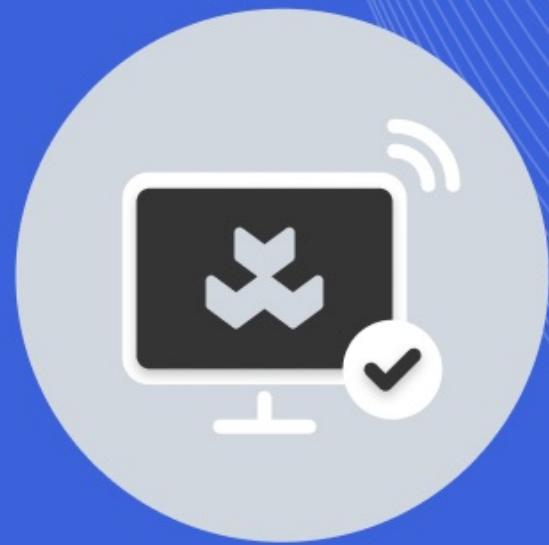
System Components



Software API and a robust driver to communicate with your device over USB, PCI Express, or the internet

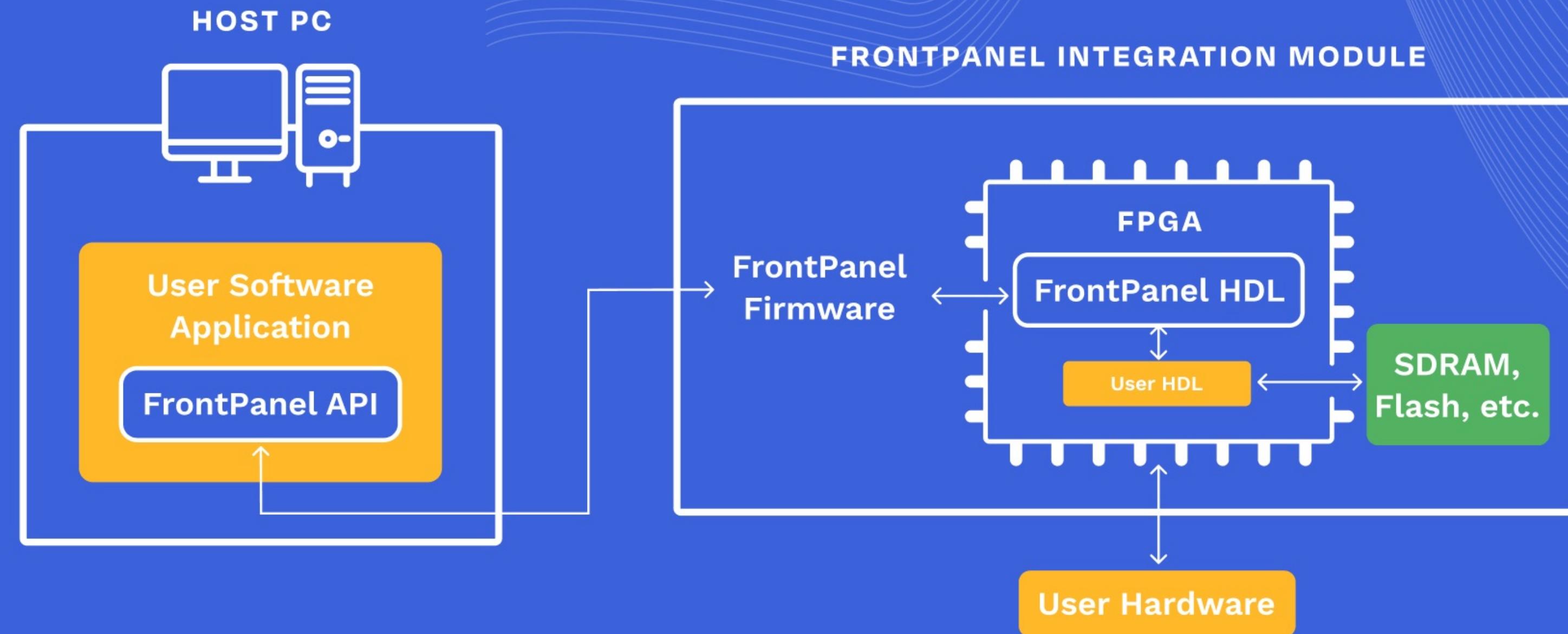


Proprietary device firmware to manage FPGA configuration and communication as well as other device management and monitoring



Lightweight FPGA IP blocks that integrate with your HDL to make host communication simple and easy

System Architecture

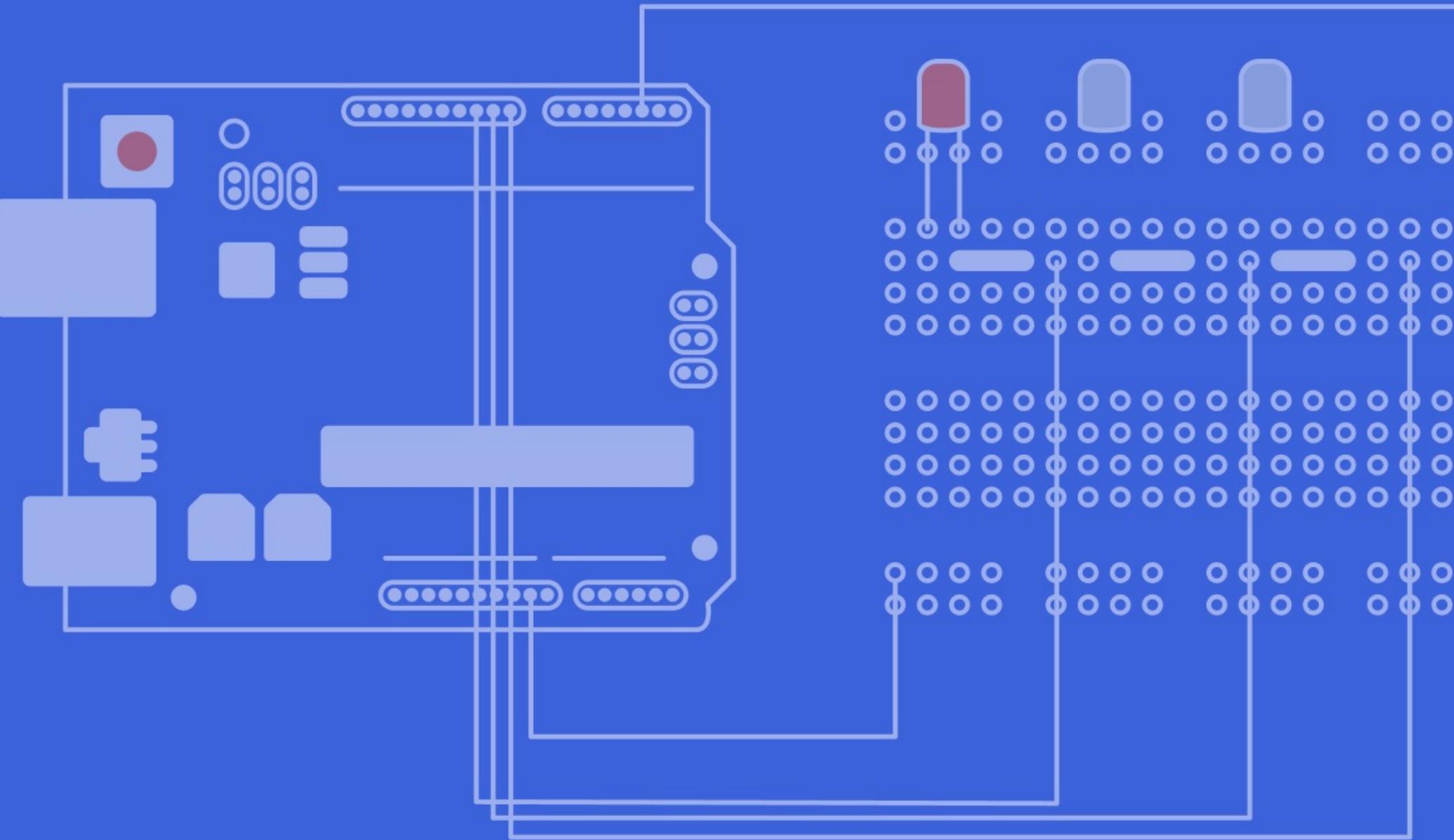


○ Provided by FrontPanel SDK

● Provided by User

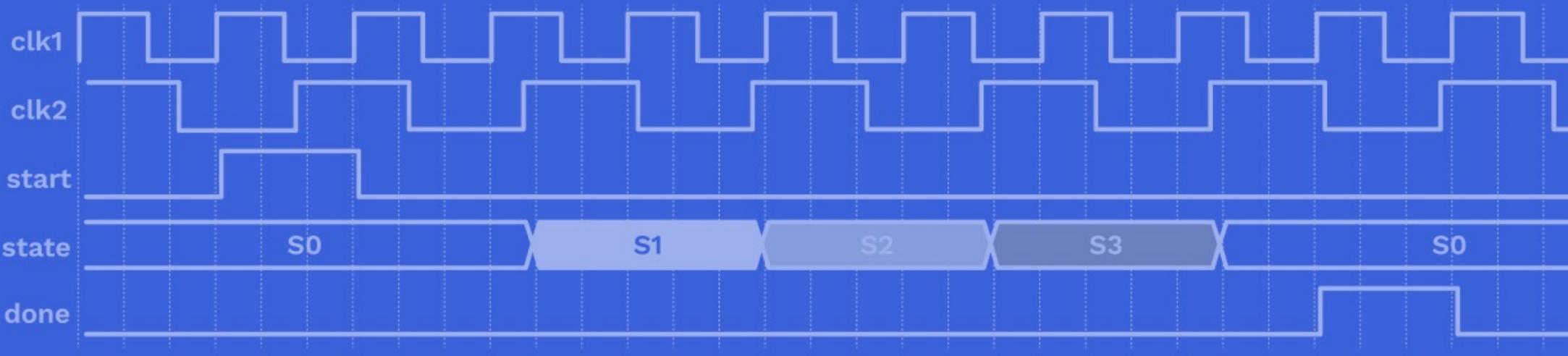
● On-Module Peripherals

Wires



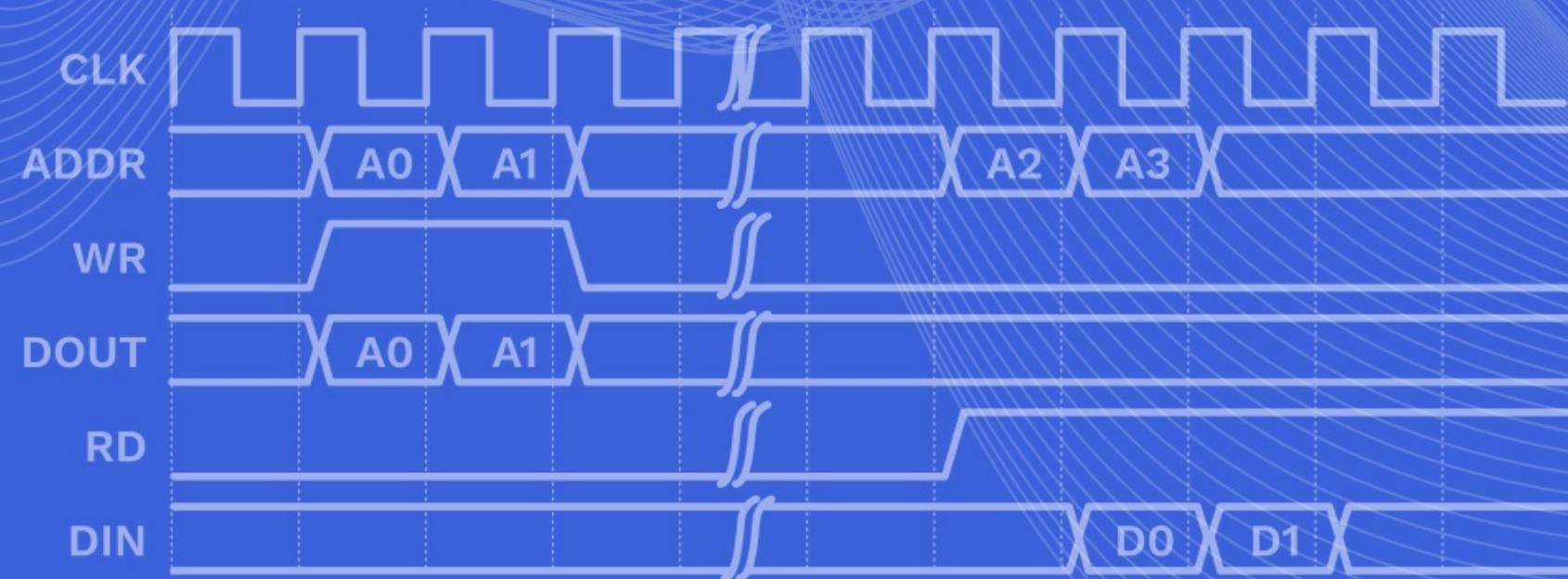
- Asynchronous - e.g. switches, pushbuttons
- 32 wires available, each is 32-bit wide
- Use synchronizers to interface to synchronous circuits reliably
- Best for asynchronous resets, data input, output monitoring

Triggers



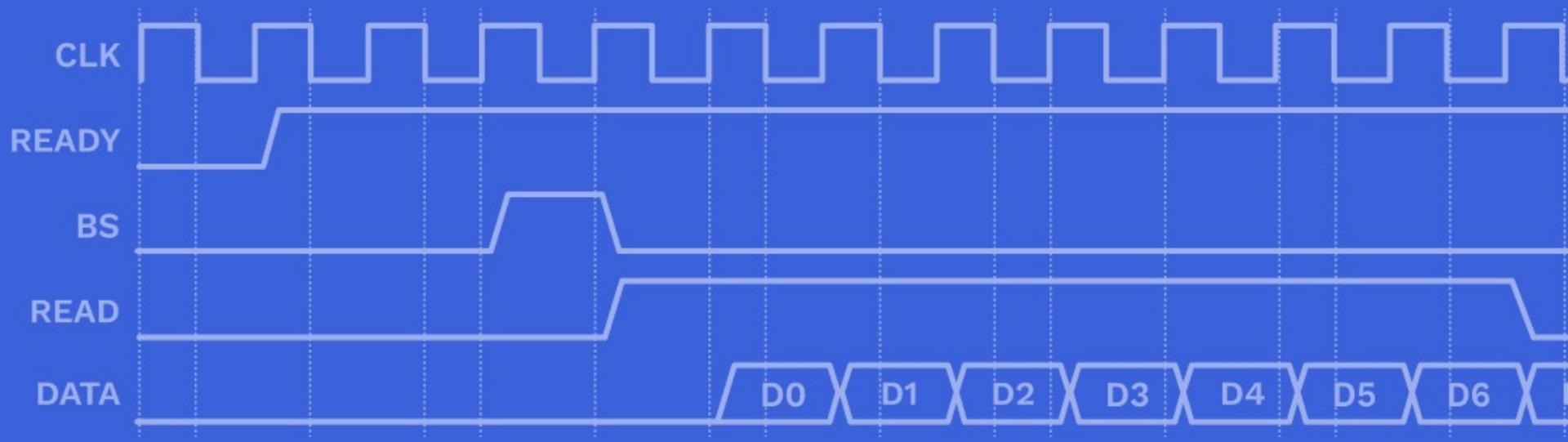
- Synchronous event / clock domain crossing
- 32 trigger bundles available, each with 32 triggers to a single clock
- Synchronizer is built-in
- Best for synchronous resets, event monitoring

Register Bridge



- Synchronous and addressable
- One register block: 32-bit data value, 32-bit address
- Good for memory interfaces, large register files, coefficient memory

Pipes



- Synchronous raw data payload transfer
- High performance data transfer to / from a single “endpoint”
- 32 pipe endpoints available, each with a 32-bit wide data bus
- Best for data acquisition, large memory transfers
- Combine with wires or triggers for advanced protocol implementations (e.g. handshaking)

Pipe Performance

- Super Speed USB: **350 MBps** sustained uni-directional transfers
- High Speed USB: **38 MBps** sustained uni-directional transfer



Performance figures represent optimal transfer conditions and may vary by host OS, host system architecture, and other factors.

Additional Features

- Product-specific **Device Settings** for volatile & non-volatile registers
- Product-specific **Device Sensors**: voltage, current, temperature monitoring
- **Reset Profiles** to initialize new-configuration FrontPanel context
- Software-programmable VIO for select modules
- SYZYGY support for selected development boards and breakout boards (including SmartVIO)



Camera Example Design



- Wires implement register settings such as frame size and capture mode
- Triggers implement capture and readout event
- Pipes implement image buffer transfer
- Internal FIFOs implement a DDR image buffer controller
- N-Deep capture controller for large capture memory

Desktop App



- Rapid user interface prototyping with virtual UI elements
- Text-based XML UI description file
- Supports wire, trigger, and pipe endpoints
- Business logic implemented in Lua scripts

- 💡 LEDs
- 🔢 Hexadecimal displays
- ScrollIndicator Sliders
- 💡 Pushbuttons
- checkbox Checkboxes
- toggle Toggle buttons
- grid Numerical entry

The screenshot shows the Opal Kelly FrontPanel application interface. On the left, a terminal window displays a portion of a Lua script. The script includes code for handling button events, setting error and status messages, and interacting with a panel named "panel1". On the right, the main window displays a virtual front panel titled "Counters Example". It features two digital counters labeled "Counter #1" and "Counter #2". Counter #1 has a 7-bit input range (x[7:4] x[3:0]) and displays the value "5 5". Counter #2 has a 7-bit input range (y[7:4] y[3:0]) and displays the value "9 A". Both counters have "Reset" and "Disable" buttons. Below the counters are "Up" and "Down" buttons, and a checkbox for "Autocount". The top left of the main window shows device information: "XEM7350-K70T", "Opal Kelly XEM7350", "Serial #14110008AQ", and "Firmware: 1.16". The bottom of the window shows the text "Welcome to FrontPanel." and "Panel #1 XEM7350-K70T".

```
-- `Write To Pipe In` button event
function OnPipeInButton(button, event)
    if not button:IsPressed() then return end

    SetError("")
    SetStatus("Writing To Pipe In...")

    local panel = okUI:FindPanel("panel1")
    m_transferSize = panel:FindDigitEntry("writeLengthBytes"):GetValue()

    Setup()
    Transfer(event:GetDevice(), 1, true);

```

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Platform Support



C++

C#

Python

Java

Javascript

3rd-party Library (e.g. MATLAB, LabView)

FPGA Modules + FrontPanel® SDK



XEM8350

Xilinx Kintex UltraScale XCKU060
4 GiB DDR4 memory with ECC
Dual SuperSpeed USB 3.0 interface
330+ I/O
28 Gigabit Transceivers



XEM7310MT

Xilinx Artix-7 XC7A75T / A200T
1 GiB DDR3 memory
SuperSpeed USB 3.0 interface
136 I/O and 4 Gigabit Transceivers
Samtec 0.5mm board-to-board connectors

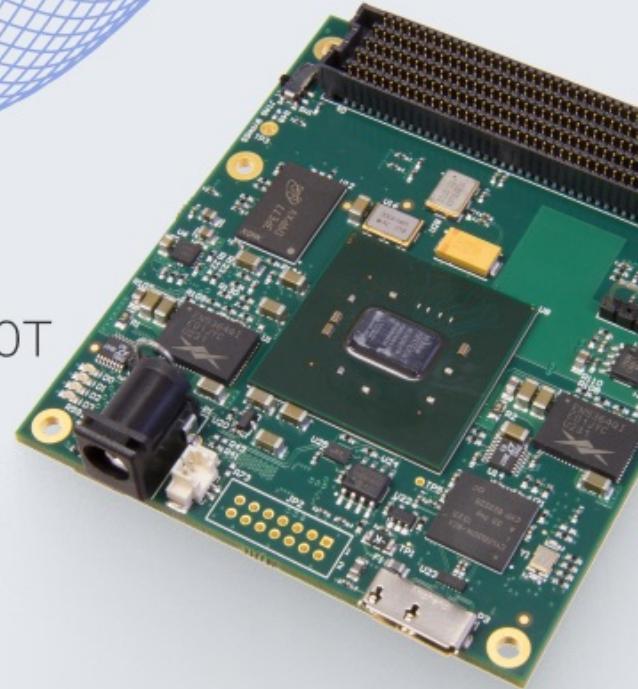


ZEM5305

Intel Cyclone V (A2)
512 MiB DDR3 memory
SuperSpeed USB 3.0 interface
94 I/O and 2 GCLK
Samtec 0.8mm Connectors

XEM7350

Xilinx Kintex-7 XC7K160T / K410T
512 MiB DDR3 memory
SuperSpeed USB 3.0 interface
170 I/O and 8 Gigabit Transceivers
FMC-HPC expansion connector

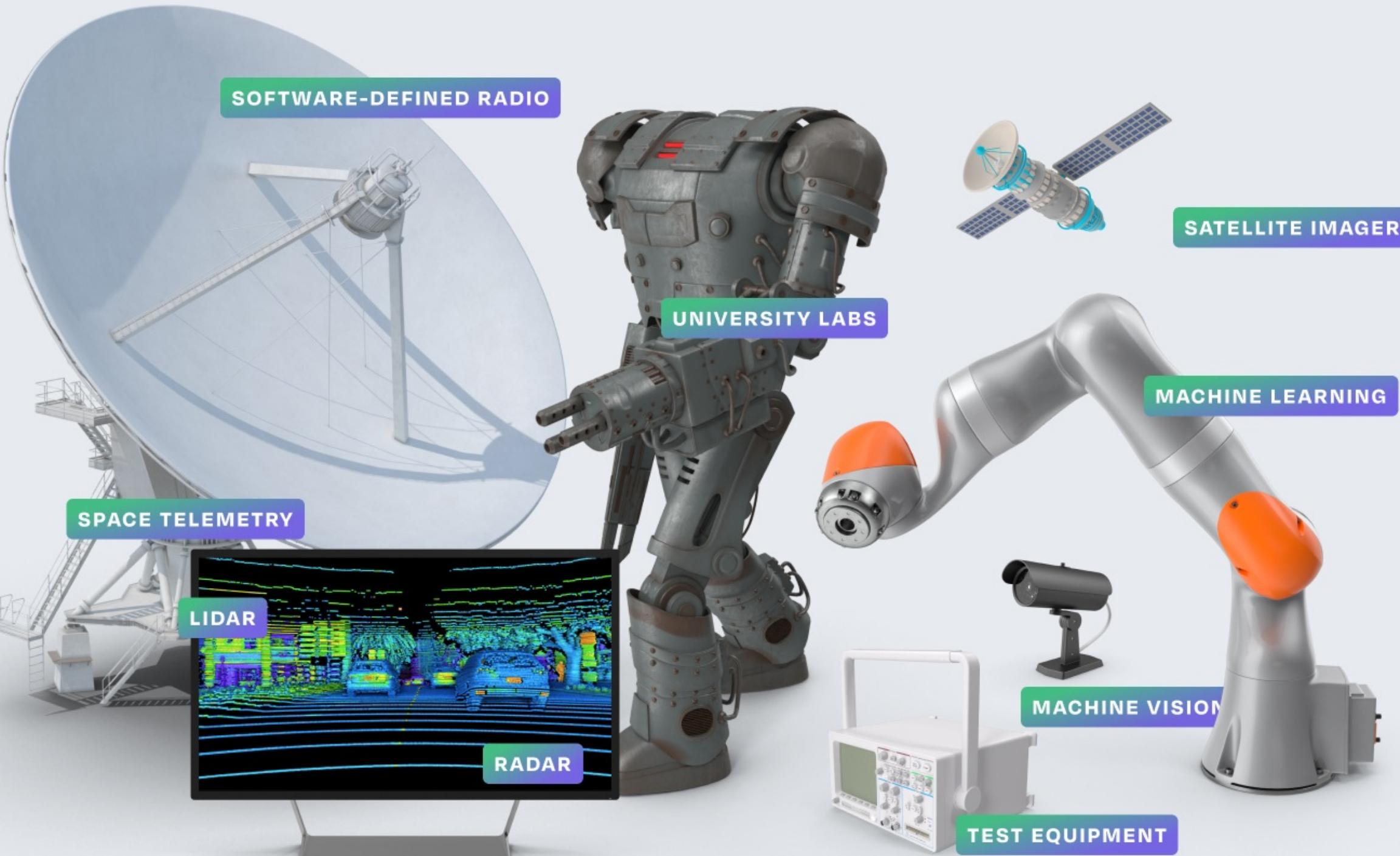


ZEM5310

Intel Cyclone V E 5CEFA4F23C7N
512 MiB DDR3 memory
SuperSpeed USB 3.0 interface
106 I/O
Samtec 0.8mm board-to-board connectors



Applications



Machine Learning / AI
Software-Defined Radio
Networking
Machine Vision
Test Equipment
University Labs
Scientific Instrumentation
Data Acquisition
RADAR, LIDAR
Satellite Imagery
Advanced / Remote Sensing
Semiconductor Simulation, Test, and Debug

FrontPanel Deployments

- Over 2,200 named customers
(+ “No Company” purchases)
- Over 200 Universities worldwide
- Research Organizations
- National Laboratories
- Military / Aerospace
- Scientific Instrumentation
- Commercial



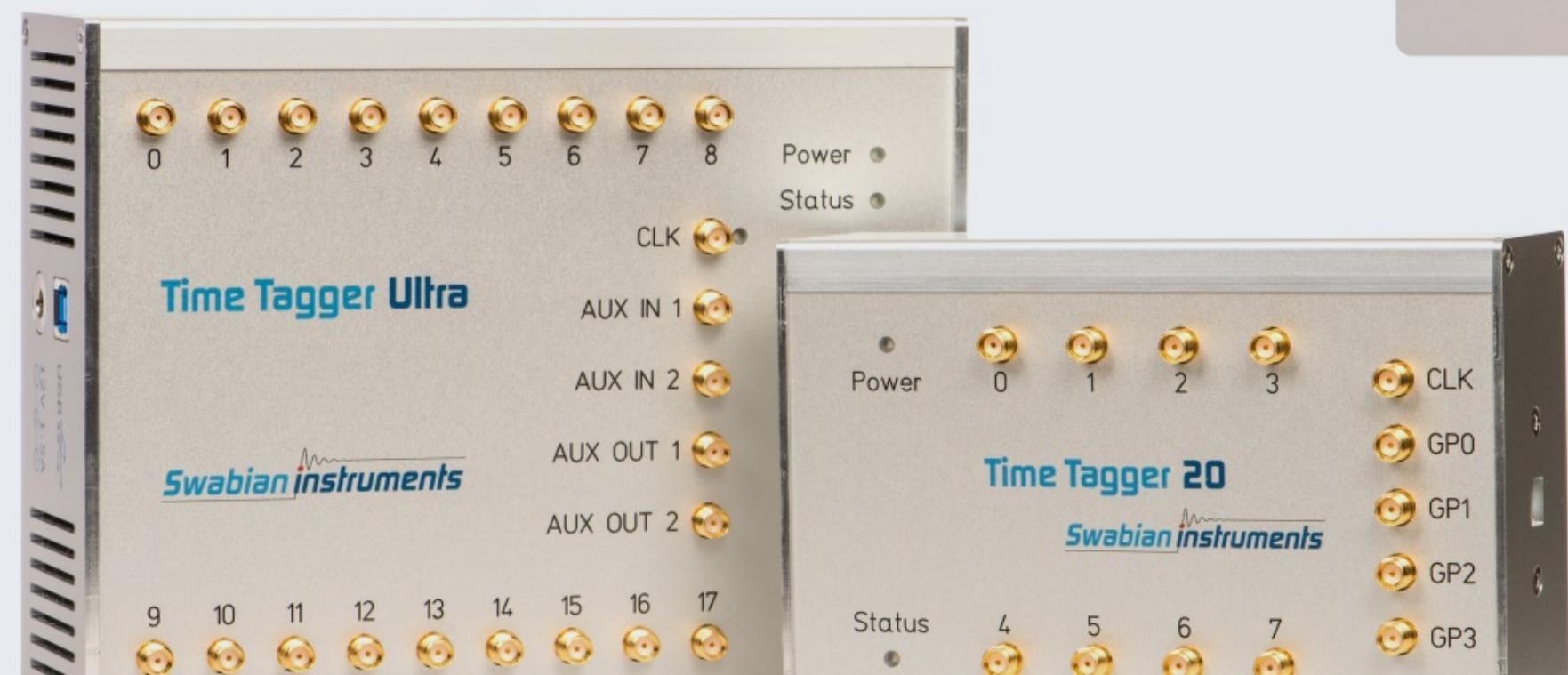
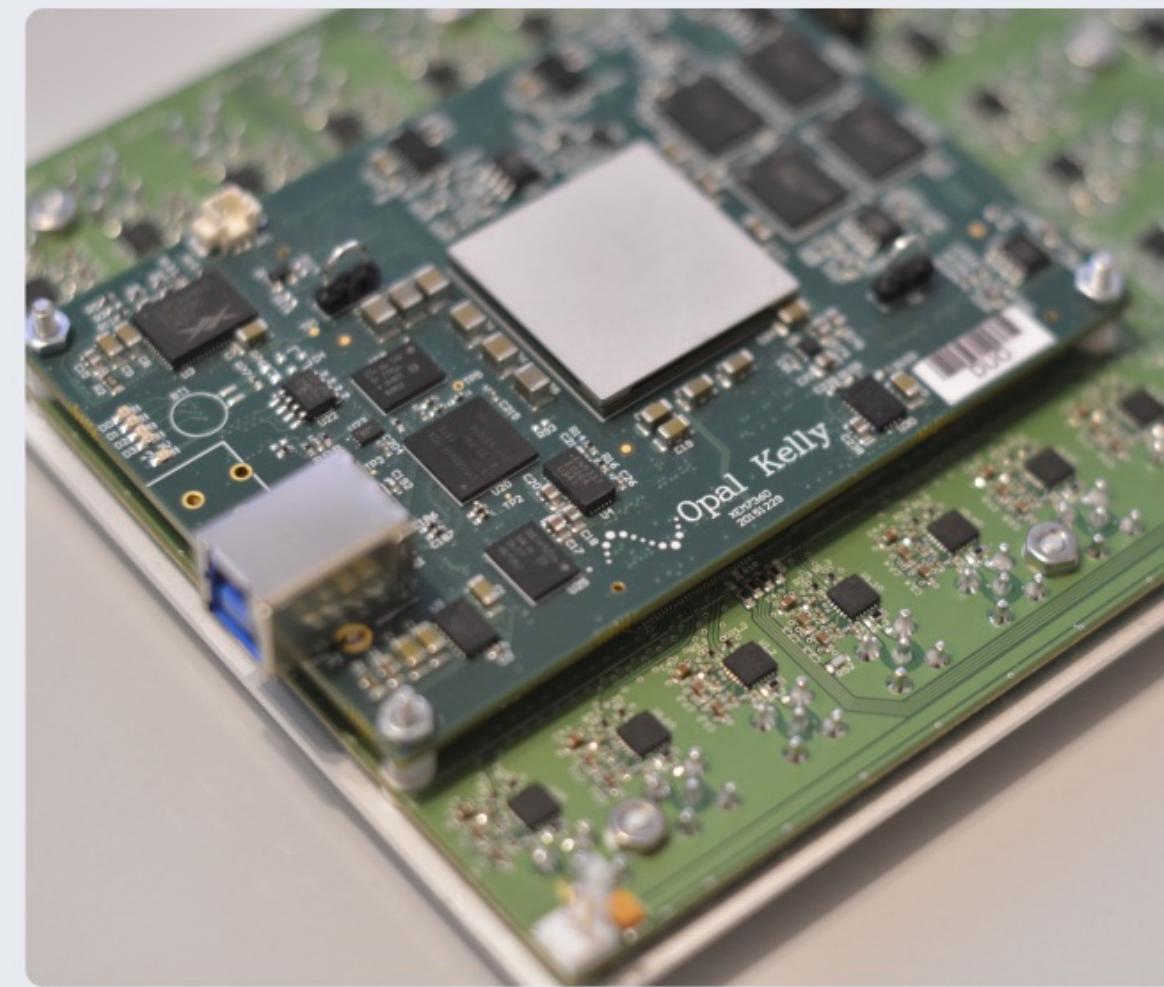
Google™



Opal Kelly

Production-Ready Customer Story: **Swabian Instruments**

- Located in Stuttgart, Germany
- Ultra high-end time tagging for photonics, quantum
- Time Tagger 20 - Based on Opal Kelly XEM3005
- Time Tagger Ultra - Based on Opal Kelly XEM7360



Key Benefits



Reduce time to market.



Build a team that strengthens your core.



Simplify your supply chain.