XEM8320
Xilinx Artix UltraScale+
FPGA Development Platform

Opal Kelly

XILINX

ARTIX
UltraSCALE+
XEM8320-AU25P

Xilinx Artix UltraScale+ AU25P
SuperSpeed USB 3.0 interface
1 GB DDR4-2400 memory
32 MiB QSPI Flash
4 SYZYGY Standard Ports
2 SYZYGY Transceiver Ports (TXR4)

Host Interface
- USB 3.0 Type C, SuperSpeed
- FrontPanel Support

FPGA
- XCAU25P-2FFVB676E

Memory
- 1 GiByte DDR4-2400, 16-bit wide data

NV Memory
- 16 MiB System Flash
- 32 MiB FPGA QSPI Flash

Clock Generation
- Three fixed-output

FPGA I/O Voltage
- Up to +3.3V

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<table>
<thead>
<tr>
<th>Feature</th>
<th>XEM8320-AU25P</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>XCAU25P-2FGG</td>
</tr>
<tr>
<td>System Logic Cells</td>
<td>308,437</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>282,000</td>
</tr>
<tr>
<td>CLB LUTs</td>
<td>141,000</td>
</tr>
<tr>
<td>Distributed RAM (max)</td>
<td>4.7 MiB</td>
</tr>
<tr>
<td>Block RAM (MiB)</td>
<td>10.5 MiB</td>
</tr>
<tr>
<td>Block RAM</td>
<td>300 blocks</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>1,200</td>
</tr>
<tr>
<td>Clock Management Tiles</td>
<td>4</td>
</tr>
<tr>
<td>GTY Transceivers (16.375 Gbps)</td>
<td>24</td>
</tr>
</tbody>
</table>
XEM8320-AU25P

Features
(Rev Cxx shown)

- 6-pin PCIE Power
- 8 - 14 VDC Power In
- Barrel Jack Power
- Power Switch
- USB Type C SuperSpeed
  Opal Kelly FrontPanel
- SYZYGY (Standard)
- 1 GiB DDR4
- SYZYGY (Transceiver - TXR4)
- JTAG (USB C)
- SYZYGY (Transceiver - TXR4)
- Artix UltraScale+ FPGA
  XCAU25P-2FFVB676E
- SMA Rx/Tx/RefClk
- 2x SFP+
- Clock Oscillators:
  - 100 MHz (fabric)
  - 150 MHz (DDR4)
  - 125 MHz (MGT)
- 256 Mib Serial QSPI Flash
- SYZYGY (Standard)
- 6 LEDs
- SYZYGY (Standard)
FrontPanel

Build high-performance software-connected FPGA applications for prototypes, proof-of-concept, and production
FrontPanel Overview
Build high-performance software-connected FPGA applications for prototypes, proof-of-concept, and production

- Turnkey high-performance SW/HW integration
- Ideal for rapid development of prototypes and proof-of-concept
- Production-ready with thousands of customer deployments
- Standalone desktop app or API for custom integration
- Lightweight FPGA footprint (low gate count)
- Behavioral simulation
FrontPanel System Components

1. Software API and a robust driver to communicate with your device over USB, PCI Express, or the internet.

2. Proprietary device firmware to manage FPGA configuration and communication as well as other device management and monitoring.

3. Lightweight FPGA IP blocks that integrate with your HDL to make host communication simple and easy.
FrontPanel API Platform Support

- C++
- C#
- Python
- Java
- Javascript

3rd-party Library (e.g. MATLAB, LabView)
FrontPanel Desktop App

- Rapid user interface prototyping with virtual UI elements
- Text-based XML UI description file
- Supports wire, trigger, and pipe endpoints
- Business logic implemented in Lua scripts

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Opal Kelly FrontPanel

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```
-- 'Write To Pipe In' button event
function OnPipeInButtonDown(button, event)
    if not button:isPressed() then return end
    SetError(""
    SetStatus("Writing To Pipe In..."

    local panel = oKUI:FindPanel("panel1")
    m_transferSize = panel:findDigitEntry("writeLengthBytes"); GetValue()
    Setup()
    Transfer(event:GetDevice(), 1, true);
```
SYZYGY Overview

- High-performance, standardized FPGA / peripheral connectivity
- Higher performance than PMOD
- Less “pin greedy” than FMC
- SmartVIO is compatible with FPGA I/O architectures
- Cable-capable and impedance controlled
SYZYGY Benefits

• Modern connectivity for data acquisition, instrumentation, and sensing
• Modular, adaptable, expandable
• Customers get further, faster
• Longer useful life of the development platform
• Learn more at SYZYGYFPGA.IO
Peripherals

Also Available...
Test Board (Standard)
Test Board (Transceiver)
6” Standard Cable
6” Transceiver Cable

From Digilent...
Zmod AWG 1411
Zmod Scope 1410

Coming Soon...
Instrumentation DAC+ADC
Camera Reference Design

- Color image sensor - 3.4 Mpixel, 60 fps, global shutter
- SDRAM-based multi-buffer image capture pipeline and memory controller
- Cross-platform C++ GUI Desktop App
- Browser-based Javascript built on FrontPanel-over-IP
- Free movement with SYZYGY cabling
- Open-source gateware and software
Data Acquisition Reference Designs

- **SZG-ADC** • 125 MSPS real-time simple oscilloscope / waveform capture
- **SZG-DAC** • 125 MSPS signal generator and digital modulator
- FrontPanel API used for control and real-time visualization
- CORDIC signal generator
- Open-source gateware and software
Ethernet Reference Design

- SZG-ENET1G - 10/100/1000 RGMII ethernet PHY (Texas Instruments DP83867)
- Xilinx Tri-Mode Ethernet MAC (TEMAC) reference design
- FrontPanel GUI for control
PCI Express Reference Design

- SZG-PCIEX4 - PCI Express Gen 3, 4-lane interface card
- Xilinx PCI Express reference design
- SYZYGY cabling for external FPGA platform
XEM8320-AU25P
Price and Availability

$1,399.95
opalkelly.com
XEM8310-AU25P SOM

- Xilinx XCAU25P-2FFVB676E FPGA
- 2 GiByte DDR4-2666, 32-bit wide data
- Single-input power supply (7.5 - 15 VDC)
- 149 FPGA I/O
- 12 GTY gigabit transceivers
- Full FrontPanel SDK / USB 3.0 support
- Software-controlled bank voltages

$1,199.95*

opalkelly.com

* Volume pricing available
Opal Kelly Incorporated

- Founded 2004 with the introduction of FrontPanel USB 2.0
- FrontPanel SDK for rapid prototyping and proof-of-concept
- Robust API and lifecycle managed modules for low- to mid-volume production
- Data acquisition • machine vision • software-defined radio • university labs • test & measurement • research-grade scientific instrumentation • RADAR • LIDAR • satellite imaging • remote sensing • HW/SW simulation
- Introduced SYZYGY connectivity standard in 2017
- ISO 9001:2015 QMS, certified 2019