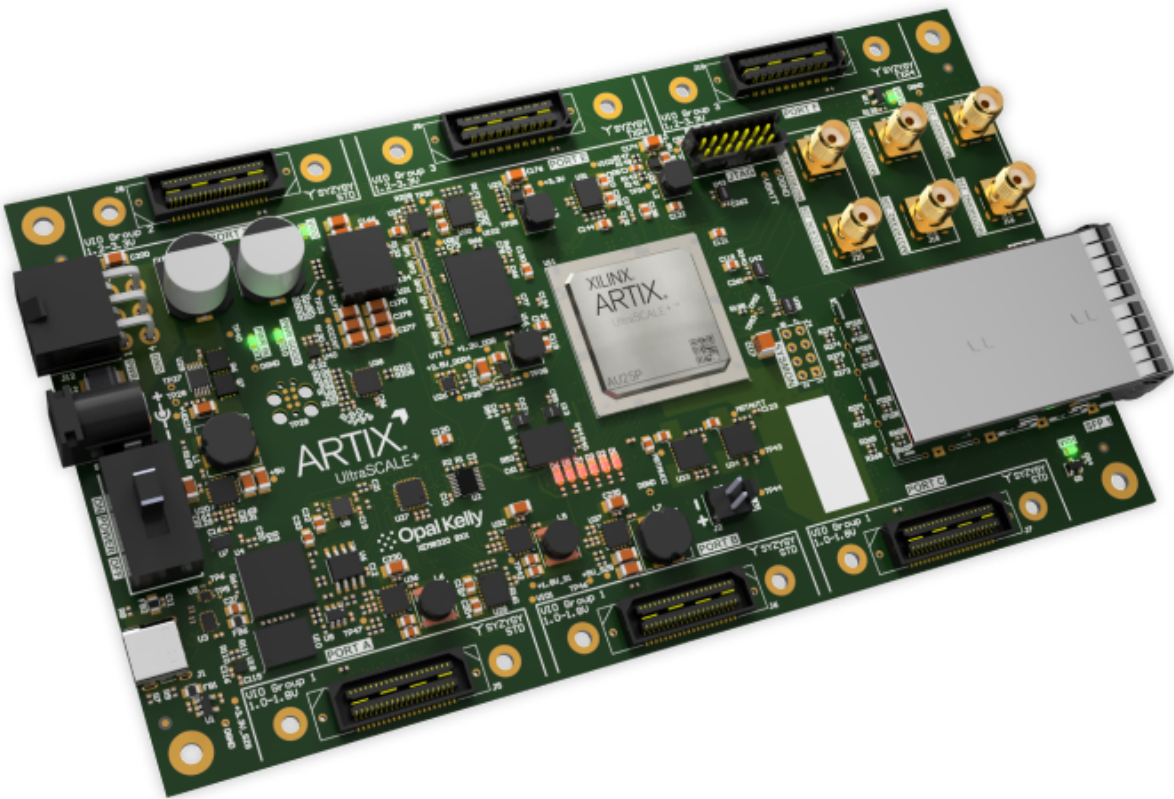


XEM8320

Xilinx Artix UltraScale+
FPGA Development Platform

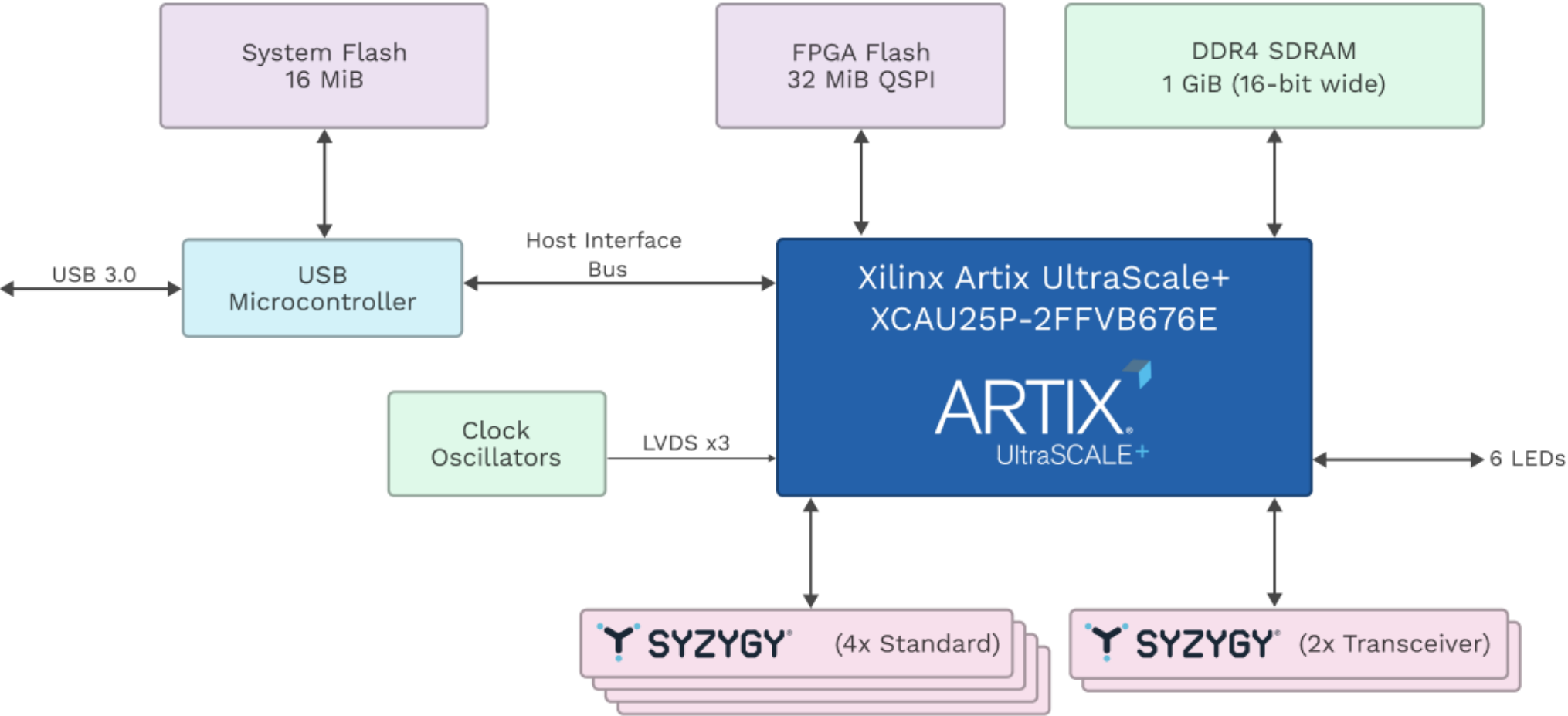
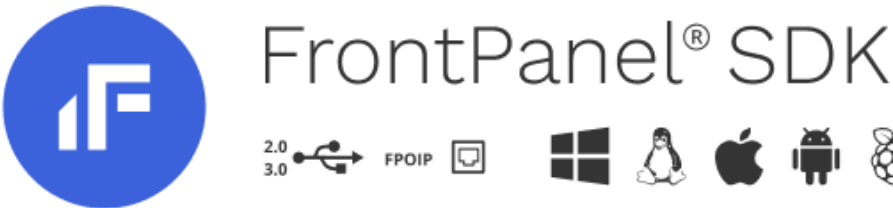


XEM8320-AU25P



Xilinx Artix UltraScale+ AU25P

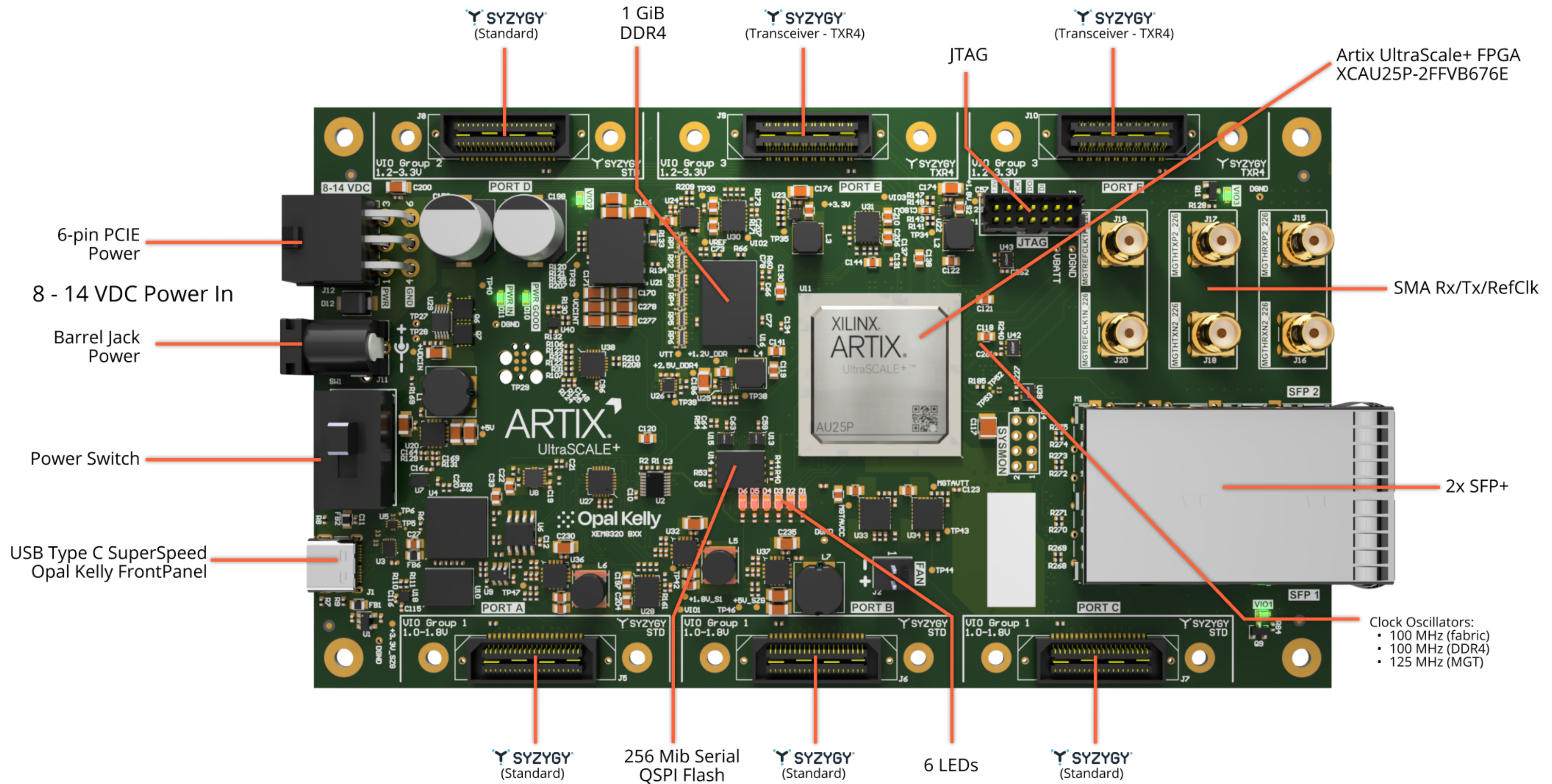
- SuperSpeed USB 3.0 interface
- 1 GiB DDR4-2666 memory
- 32 MiB QSPI Flash
- 4 SYZYGY Standard Ports
- 2 SYZYGY Transceiver Ports (TXR4)



Host Interface	USB 3.0 Type C, SuperSpeed FrontPanel Support
FPGA	XCAU25P-2FFVB676E
Memory	1 GiByte DDR4-2666, 16-bit wide data
NV Memory	16 MiB System Flash 32 MiB FPGA QSPI Flash
Clock Generation	Three fixed-output
FPGA I/O Voltage	Up to +3.3V

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC Input	+8.0		+14.0	VDC
DC Input Ripple	-	-	50	mVp-p
Operating Temperature	0	-	+70	°C
Storage Temperature	-50	-	+100	°C
Weight		125		grams
Clock Frequency		100 / 100 / 125		MHz
Clock Jitter		0.5		ps RMS

FEATURE	XEM8320-AU25P
FPGA	XCAU25P-2FGG
System Logic Cells	308,437
CLB Flip-Flops	282,000
CLB LUTs	141,000
Distributed RAM (max)	4.7 Mib
Block RAM (Mib)	10.5 Mib
Block RAM	300 blocks
DSP Slices	1,200
Clock Management Tiles	4
GTy Transceivers (16.375 Gbps)	24





FrontPanel

Build high-performance software-connected FPGA applications for
prototypes, proof-of-concept, and production

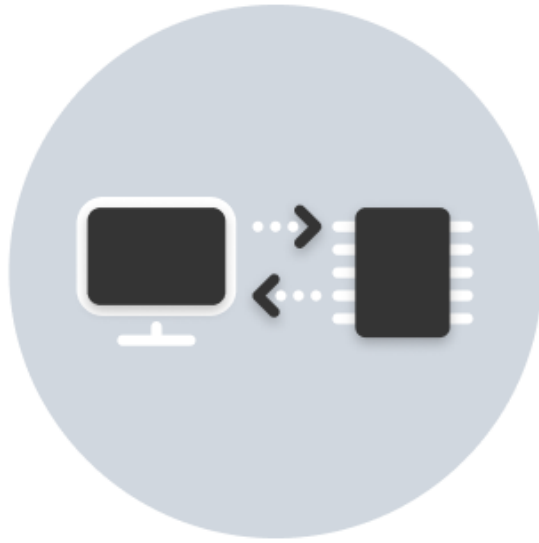


FrontPanel Overview

Build high-performance software-connected FPGA applications for prototypes, proof-of-concept, and production

- Turnkey high-performance SW/HW integration
- Ideal for rapid development of prototypes and proof-of-concept
- Production-ready with thousands of customer deployments
- Standalone desktop app or API for custom integration
- Lightweight FPGA footprint (low gate count)
- Behavioral simulation

FrontPanel System Components



Software API and a robust driver to communicate with your device over USB, PCI Express, or the internet



Proprietary device firmware to manage FPGA configuration and communication as well as other device management and monitoring



Lightweight FPGA IP blocks that integrate with your HDL to make host communication simple and easy

FrontPanel API Platform Support



C++

C#

Python

Java

Javascript

3rd-party Library (e.g. MATLAB, LabView)

FrontPanel Desktop App



- Rapid user interface prototyping with virtual UI elements
- Text-based XML UI description file
- Supports wire, trigger, and pipe endpoints
- Business logic implemented in Lua scripts



LEDs



Hexadecimal displays



Sliders



Pushbuttons



Checkboxes



Toggle buttons



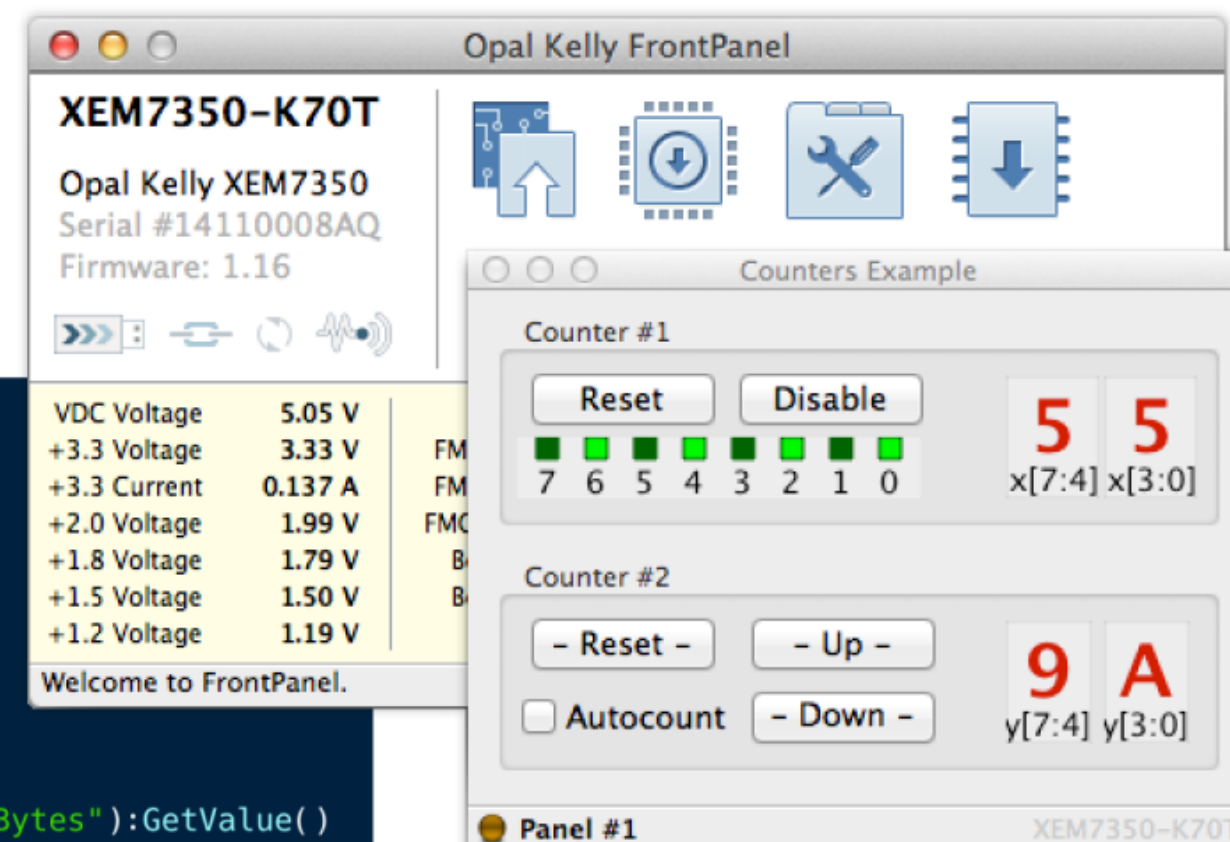
Numerical entry

```
-- 'Write To Pipe In' button event
function OnPipeInButton(button, event)
    if not button:IsPressed() then return end

    SetError("")
    SetStatus("Writing To Pipe In...")

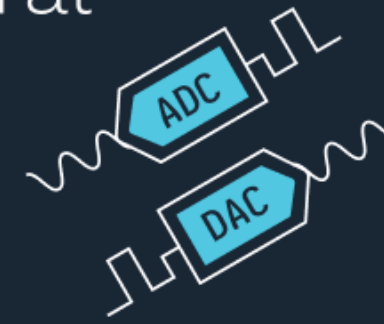
    local panel = okUI:FindPanel("panel1")
    m_transferSize = panel:FindDigitEntry("writeLengthBytes"):GetValue()

    Setup()
    Transfer(event:GetDevice(), 1, true);
```

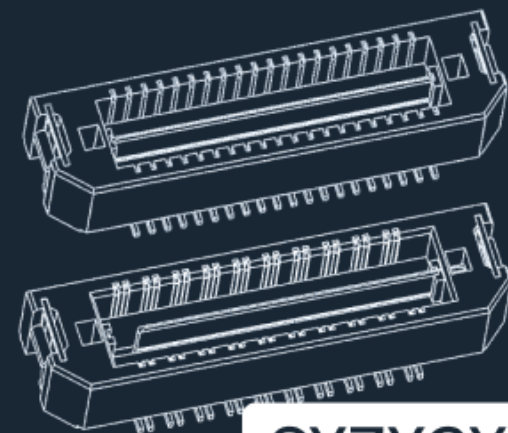


SYZYGY Overview

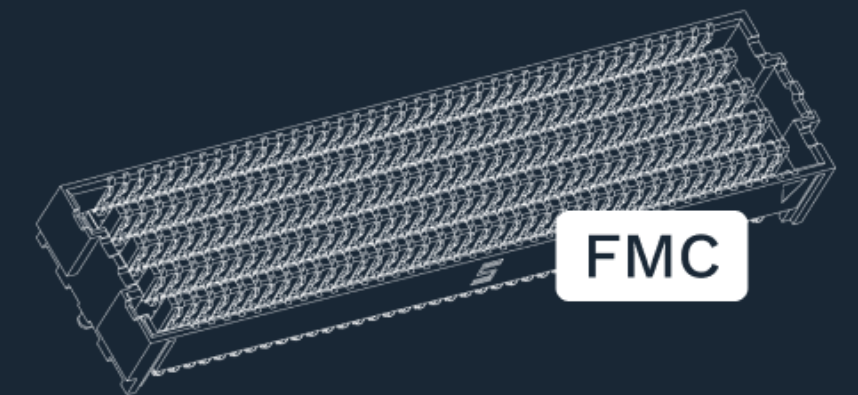
- High-performance, standardized FPGA / peripheral connectivity
- Higher performance than PMOD
- Less “pin greedy” than FMC
- SmartVIO is compatible with FPGA I/O architectures
- Cable-capable and impedance controlled



PMOD



SYZYGY



FMC

SYZYGY Benefits

- Modern connectivity for data acquisition, instrumentation, and sensing
- Modular, adaptable, expandable
- Customers get further, faster
- Longer useful life of the development platform
- Learn more at **SYZYGYFPGA.IO**



Peripherals

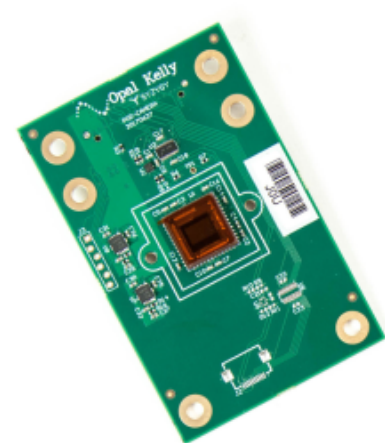
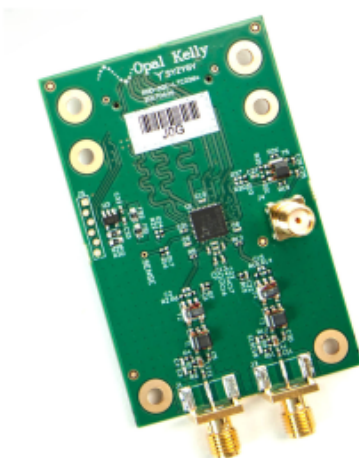
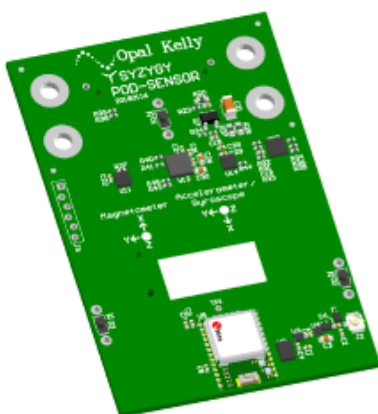


Image Sensor
3.4 Mpx, 60fps



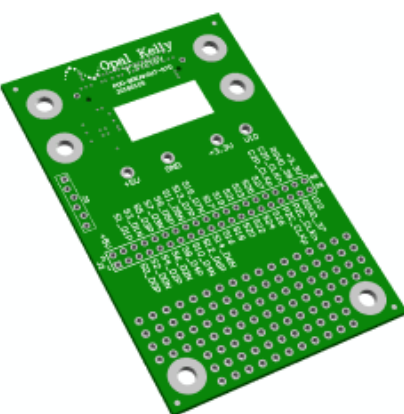
Analog-to-Digital
Dual 40 MSPS, 12-bit



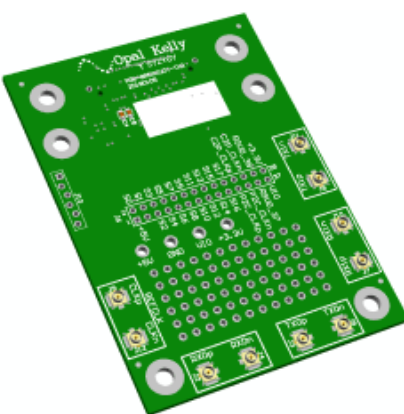
Multi-Sensor
GPS, motion, light



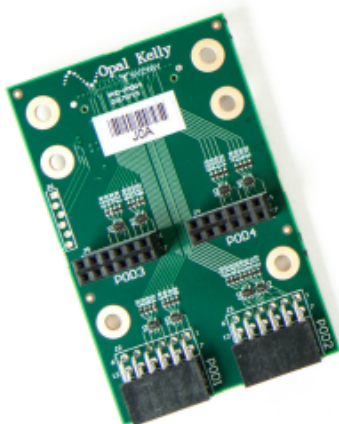
Digital-to-Analog
Dual 125 MSPS, 12-bit



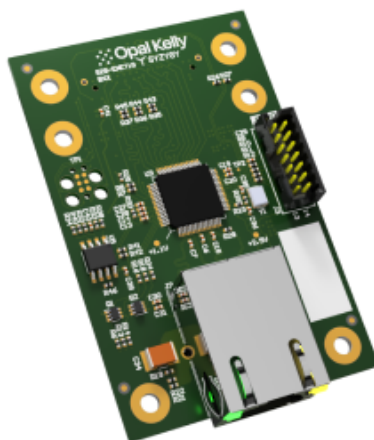
Breakout
(Standard)



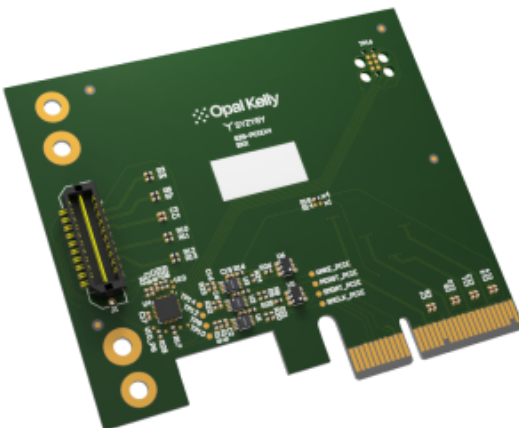
Breakout
(Transceiver)



Digilent PMOD
x4



Ethernet
10/100/1G - RJ-45



PCI Express (x4)

Also Available...

- Test Board (Standard)
- Test Board (Transceiver)
- 6" Standard Cable
- 6" Transceiver Cable

From Digilent...

- Zmod AWG 1411
- Zmod Scope 1410

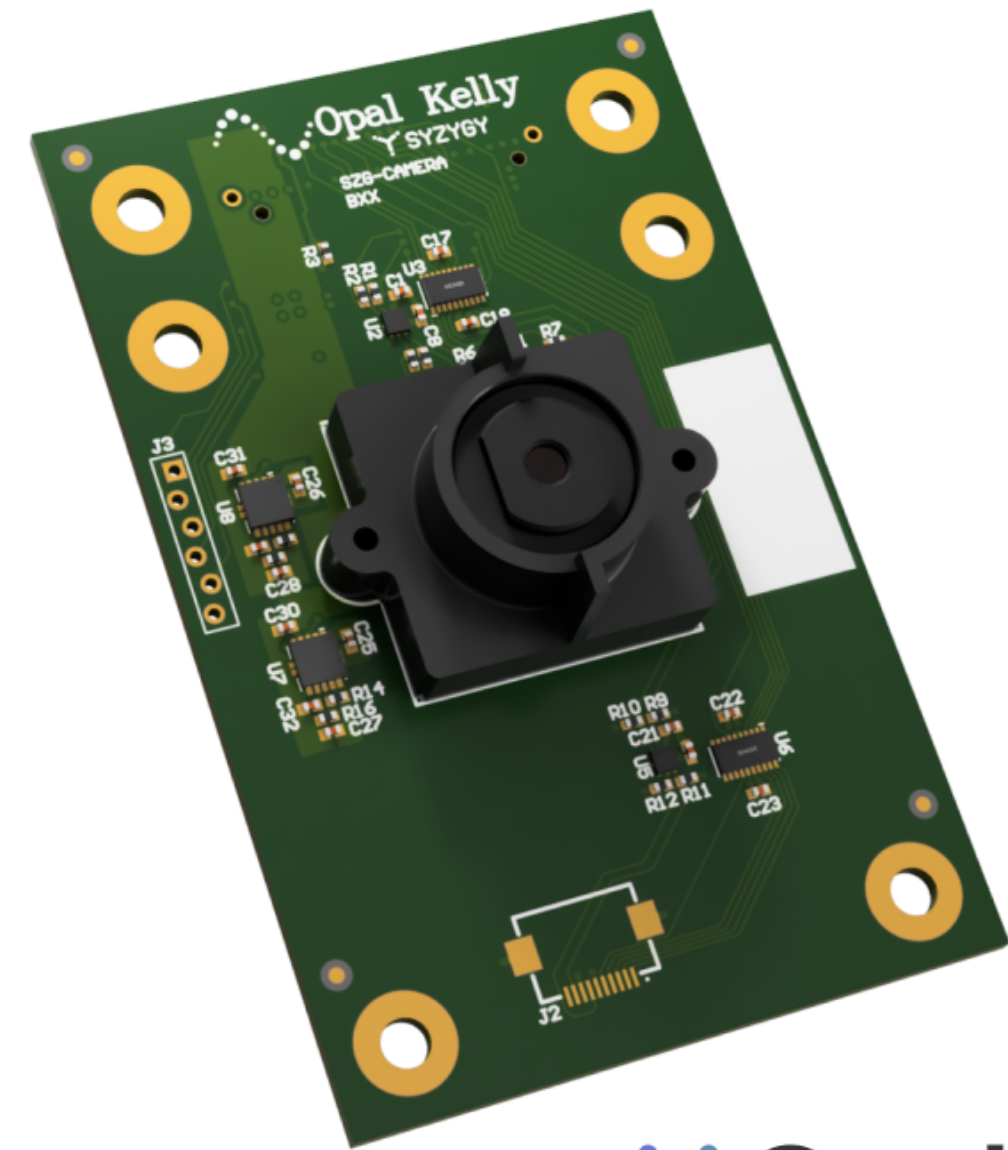
Coming Soon...

- PCI Express (x4)
- Instrumentation DAC+ADC

Camera Reference Design



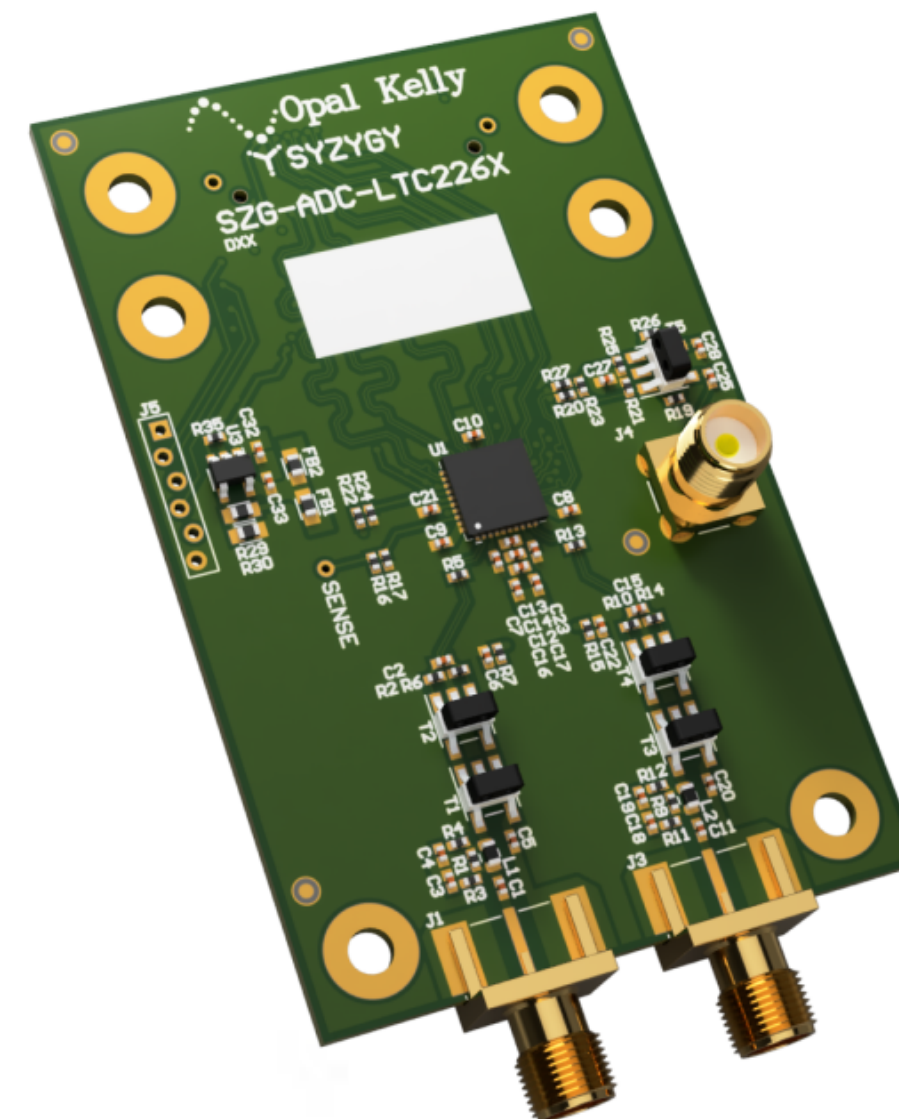
- Color image sensor - 3.4 Mpixel, 60 fps, global shutter
- SDRAM-based multi-buffer image capture pipeline and memory controller
- Cross-platform C++ GUI Desktop App
- Browser-based Javascript built on FrontPanel-over-IP
- Free movement with SYZYGY cabling
- Open-source gateway and software



Data Acquisition Reference Designs



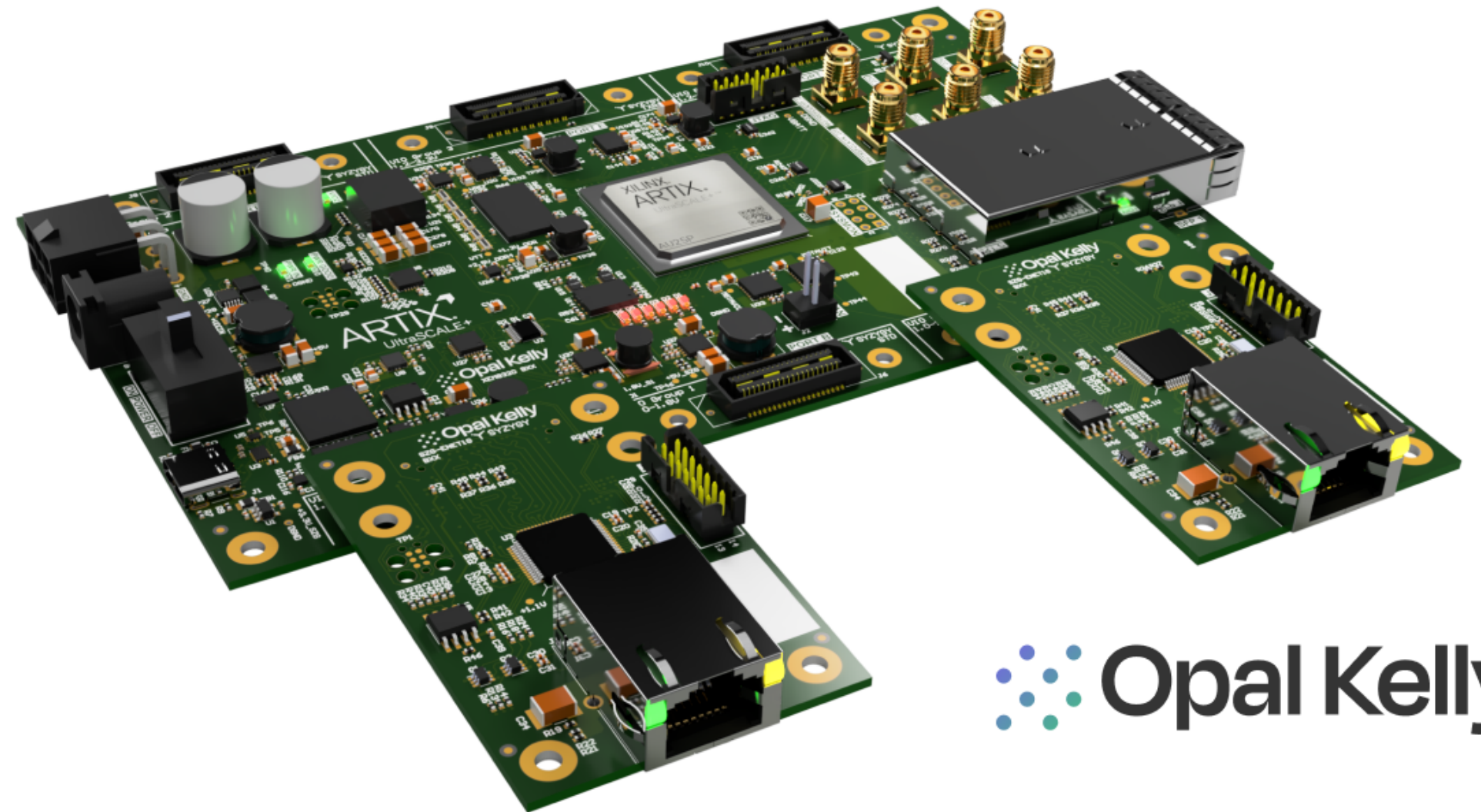
- SZG-ADC • 125 MSPS real-time simple oscilloscope / waveform capture
- SZG-DAC • 125 MSPS signal generator and digital modulator
- FrontPanel API used for control and real-time visualization
- CORDIC signal generator
- Open-source gateway and software



Ethernet Reference Design



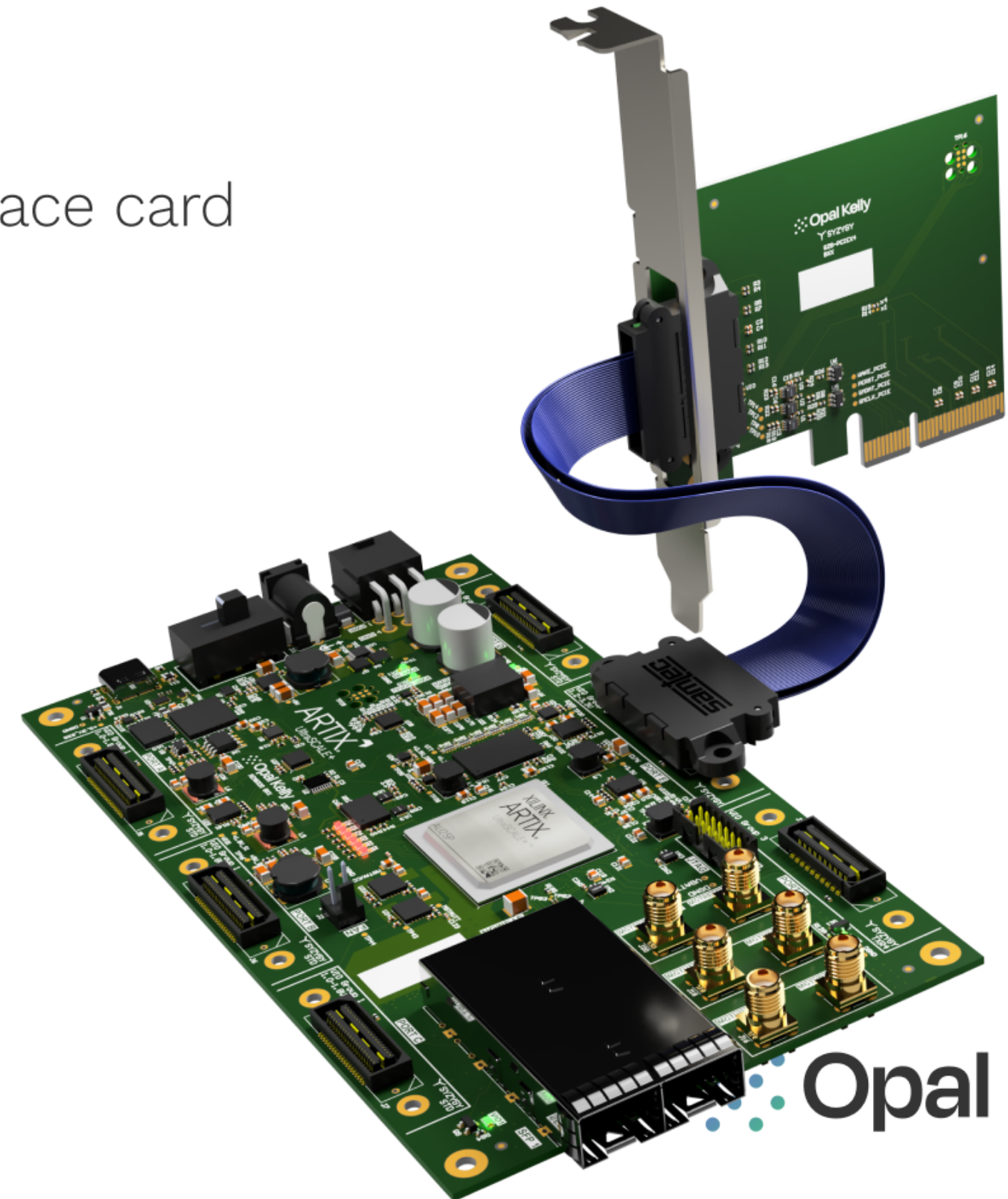
- SZG-ENET1G - 10/100/1000 RGMII ethernet PHY (Texas Instruments DP83867)
- Xilinx Tri-Mode Ethernet MAC (TEMAC) reference design
- FrontPanel GUI for control



PCI Express Reference Design



- SZG-PCIEX4 - PCI Express Gen 3, 4-lane interface card
- Xilinx PCI Express reference design
- SYZYGY cabling for external FPGA platform



XEM8320-AU25P

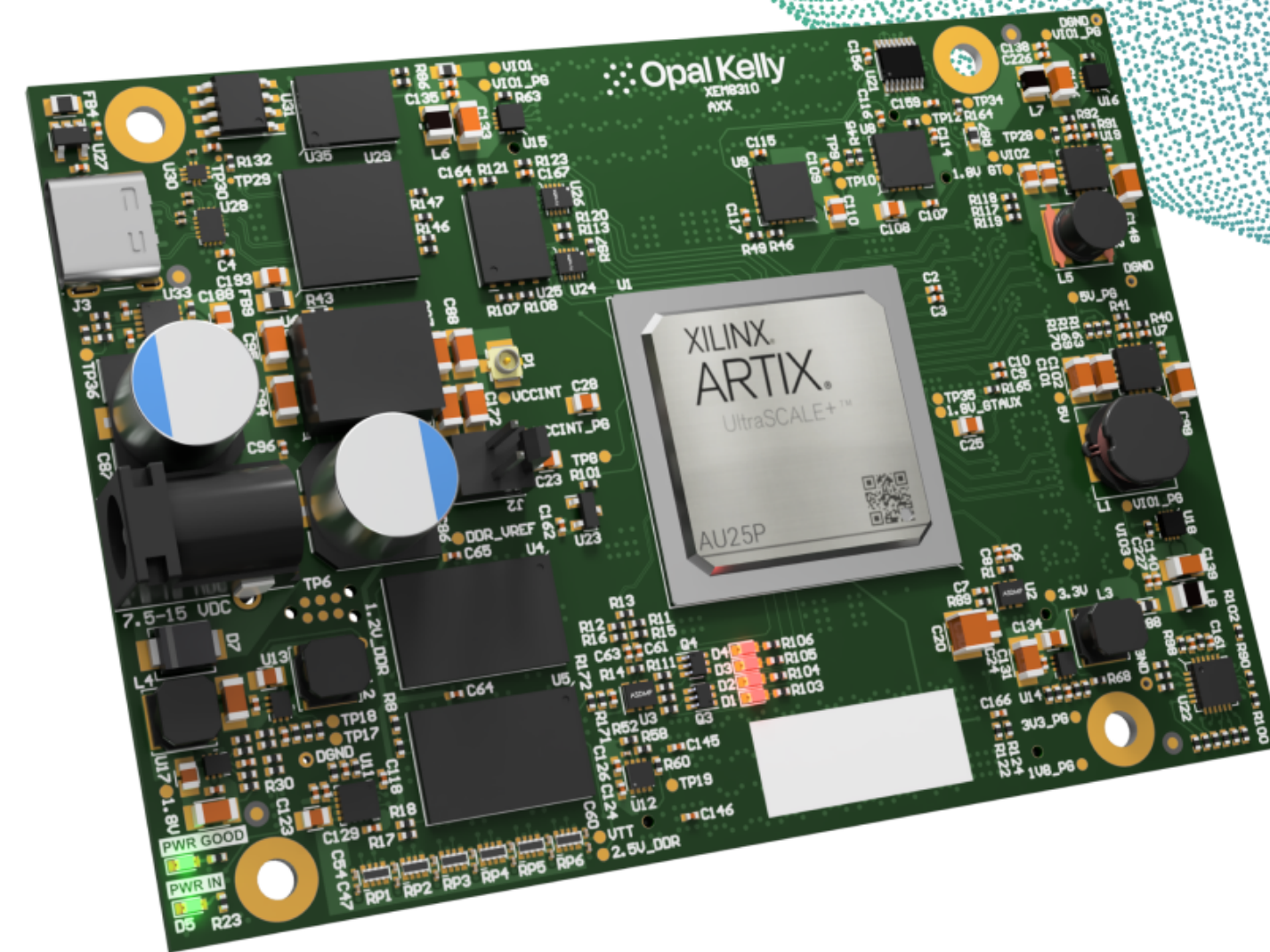
Price and Availability

\$1,349.95

opalkelly.com

XEM8310-AU25P SOM

- Xilinx XCAU25P-2FFVB676E FPGA
- 2 GiByte DDR4-2666, 32-bit wide data
- Single-input power supply (7.5 - 15 VDC)
- 149 FPGA I/O
- 12 GTY gigabit transceivers
- Full FrontPanel SDK / USB 3.0 support
- Software-controlled bank voltages



Coming Soon

opalkelly.com

Opal Kelly Incorporated

- Founded 2004 with the introduction of FrontPanel USB 2.0
- FrontPanel SDK for rapid prototyping and proof-of-concept
- Robust API and lifecycle managed modules for low- to mid-volume production
- Data acquisition • machine vision • software-defined radio • university labs • test & measurement • research-grade scientific instrumentation • RADAR • LIDAR • satellite imaging • remote sensing • HW/SW simulation
- Introduced SYZYGY connectivity standard in 2017
- ISO 9001:2015 QMS, certified 2019